19-2689; Rev 0; 1/03

MAXIM

Bus LVDS 3.3V Single Transceiver

MAX9163

General Description

The MAX9163 high-speed bus low-voltage differential signaling (BLVDS) transceiver is designed specifically for heavily loaded multipoint bus applications. The MAX9163 operates from a single 3.3V power supply, and is pin compatible with the DS92LV010A. The transceiver consists of one differential BLVDS line driver and one LVDS receiver. The driver output and receiver input are connected internally to minimize bus loading. The individual enable logic inputs (DE, $\overline{RE}$) are used to enable the driver or the receiver.

The MAX9163 driver output uses a current-steering configuration to generate a 9mA (typ) drive current. The driver accepts a single-ended input and translates it to a differential output level of 243mV (typ) into 27Ω at speeds up to 200Mbps. The MAX9163 receiver detects a differential input as low as 100mV and translates it to a single-ended output at speeds up to 200Mbps. The receiver input features a fail-safe circuit that sets the receiver output high when the receiver inputs are undriven and open, terminated, or shorted.

The MAX9163 is offered in an 8-lead SO package, and is specified for operation from -40°C to +85°C.

Applications

Cell-Phone Base Stations
Add/Drop Muxes
Digital Cross-Connects
DSLAMs
Network Switches/Routers
Backplane Interconnect
Clock Distribution

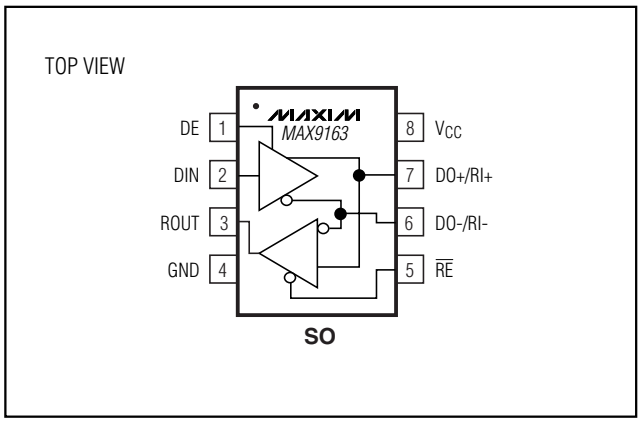
Features

- ♦ **BLVDS Signaling**
- ♦ **3.3V Operation**
- ♦ **Low-Power CMOS Design**
- ♦ **200Mbps Data-Signaling Rate**
- ♦ **±1V Common-Mode Range**
- ♦ **±100mV Receiver Sensitivity**
- ♦ **Flow-Through Pinout**
- ♦ **Receiver Output High for Undriven Open, Short, or Terminated Input**
- ♦ **8-Lead SO Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9163ESA	-40°C to +85°C	8 SO

Pin Configuration



Typical Application Circuit appears at end of data sheet.

Bus LVDS 3.3V Single Transceiver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
DO+/RI+, DO-/RI- to GND .....-0.3V to +4.0V
DIN, ROUT, DE, $\overline{RE}$ to GND .....-0.3V to (V_{CC} + 0.3V)
Driver Short-Circuit Current .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
HBM (1.5kΩ, 100pF),
DO+/RI+, DO-/RI-, DIN, ROUT, DE, $\overline{RE}$.....> ±2kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, $\overline{RE}$ = 0, $|V_{ID}|$ = 0.1V to 2.9V, common-mode input voltage (V_{CM}) = $|V_{ID}/2|$ to 3.0V - $|V_{ID}|/2$, R_L = 27Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN, DE, $\overline{RE}$)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Current	I_{IN}	$\overline{RE}$, DE, DIN = high or low	-10		+10	µA
Input Diode Clamp Voltage	V_{CL}	I_{CLAMP} = -18mA	-1.5			V
DRIVER OUTPUT (DO+/RI+, DO-/RI-)						
Differential Output Voltage	V_{OD}	Figure 1	180	250	360	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1		0.2	25	mV
Offset Voltage	V_{OS}	Figure 1	1.00	1.28	1.65	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1		1.4	25	mV
Output Short-Circuit Current	I_{OSD}	DO+/RI+ = 0, DIN = V_{CC}		-9	-20	mA
		DO-/RI- = 0, DIN = 0		-9	-20	
Output Capacitance	C_{OUT}	Capacitance from DO+/RI+ or DO-/RI- to GND		6.9		pF
RECEIVER INPUT (DO+/RI+, DO-/RI-)						
Differential Input High Threshold	V_{TH}	DE = low			100	mV
Differential Input Low Threshold	V_{TL}	DE = low	-100			mV
Input Current	I_{IN}	DE = low, V_{CC} = 0 or 3.6V; DO+/RI+, DO-/RI- = 2.4V or 0; Figure 6	-20		+20	µA
RECEIVER OUTPUT (ROUT)						
Output High Voltage	V_{OH}	V_{ID} = +100mV; I_{OH} = -400µA, DE = Low	2.90	3.28		V
		Inputs open; I_{OH} = -400µA, DE = Low	2.90	3.28		
		Inputs shorted; I_{OH} = -400µA, DE = Low	2.90	3.28		
		Inputs terminated, R_L = 27Ω; I_{OH} = -400µA, DE = Low	2.90	3.28		
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{ID} = -100mV, DE = low		0.025	0.4	V
Output Short-Circuit Current	I_{OS}	V_{ID} = +100mV, ROUT = 0, DE = low	-5	-25	-85	mA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, $\overline{RE}$ = 0, $|V_{ID}|$ = 0.1V to 2.9V, common-mode input voltage (V_{CM}) = $|V_{ID}/2|$ to 3.0V - $|V_{ID}|/2$, R_L = 27Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Supply Current	I_{CC}	DE = V_{CC}, $\overline{RE}$ = 0		13.3	20	mA
Driver Supply Current	I_{CCD}	DE = $\overline{RE}$ = V_{CC}		13.3	20	mA
Receiver Supply Current	I_{CCR}	DE = $\overline{RE}$ = 0		4.4	8	mA
Disable Supply Current	I_{CCZ}	DE = 0, $\overline{RE}$ = V_{CC}		4.4	7.5	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, R_L = 27Ω ±1%, C_L = 10pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER, DE = $\overline{RE}$ = V_{CC}						
Differential High-to-Low Propagation Delay	t_{PHLD}	Figure 2	1.0	3.2	5.0	ns
Differential Low-to-High Propagation Delay	t_{PLHD}	Figure 2	1.0	3.0	5.0	ns
Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$	t_{SKD}	Figure 2		0.2	1.0	ns
Rise Time	t_{TLHD}	Figure 2		0.8	2.0	ns
Fall Time	t_{THLD}	Figure 2		0.6	2.0	ns
Disable Time High to Z	t_{PHZ}	Figure 3	0.5	2.2	9.0	ns
Disable Time Low to Z	t_{PLZ}	Figure 3	0.5	2.2	10.0	ns
Enable Time Z to High	t_{PZH}	Figure 3	2.0	3.2	7.0	ns
Enable Time Z to Low	t_{PZL}	Figure 3	1.0	3.2	9.0	ns
RECEIVER, DE = $\overline{RE}$ = 0						
Differential High-to-Low Propagation Delay	t_{PHL}	Figure 4	2.5	6.4	12.0	ns
Differential Low-to-High Propagation Delay	t_{PLH}	Figure 4	2.5	6.0	10.0	ns
Differential Skew $\lvert t_{PHL} - t_{PLH} \rvert$	t_{SKD}	Figure 4		0.4	2.0	ns
Rise Time	t_{TLH}	Figure 4		1.0	4.0	ns
Fall Time	t_{THL}	Figure 4		0.4	4.0	ns
Disable Time High to Z	t_{PHZ}	Figure 5	2.0	5.0	6.0	ns
Disable Time Low to Z	t_{PLZ}	Figure 5	2.0	4.4	7.0	ns
Enable Time Z to High	t_{PZH}	Figure 5	2.0	4.6	13.0	ns
Enable Time Z to Low	t_{PZL}	Figure 5	2.0	4.3	10.0	ns

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to device ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 3: C_L includes probe and jig capacitance.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: Generator waveforms for all tests unless otherwise specified: f = 100MHz, Z_0 = 50Ω, t_R = t_F = 6.0ns (0 to 3V, 0% to 100%) for DE and $\overline{RE}$, t_R = t_F = 3.0ns (0 to 3V, 0% to 100%) for DIN, and t_R = t_F = 1.0ns ($|V_{ID}|$ = 0.2V, 20% to 80%) for DO+/RI+ and DO-/RI- inputs.

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Test Circuits/Timing Diagrams

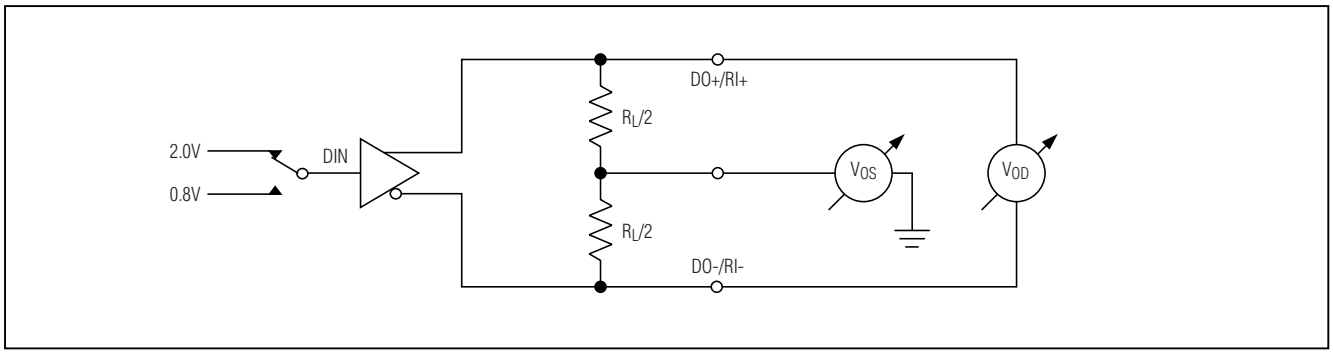


Figure 1. Differential Driver DC Test Circuit

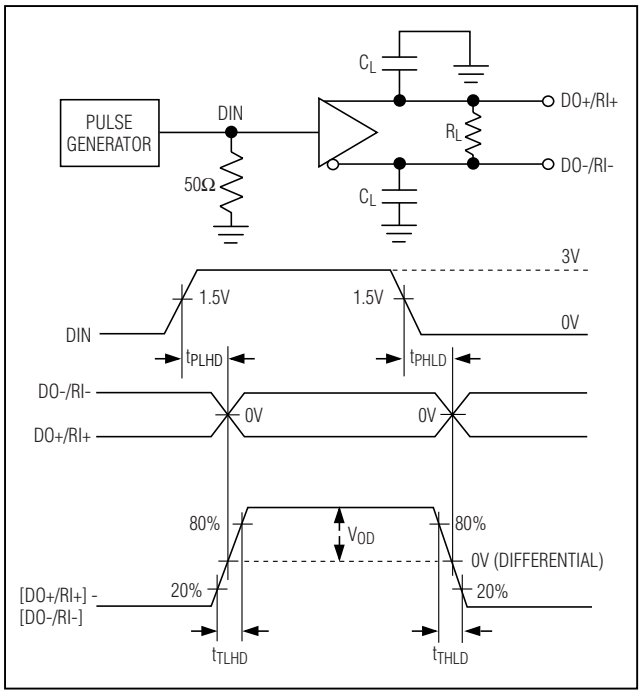


Figure 2. Driver Differential Propagation Delay and Transition Time Test Circuit and Waveforms

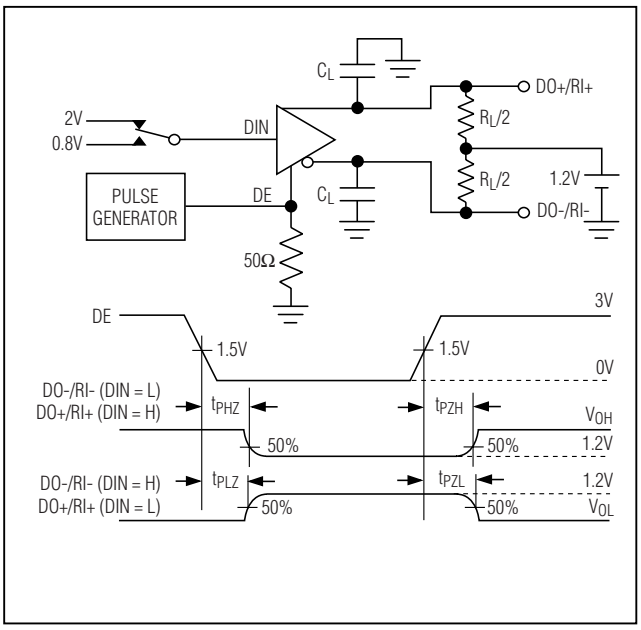


Figure 3. Driver High-Impedance Delay Test Circuit and Waveforms

Test Circuits/Timing Diagrams (continued)

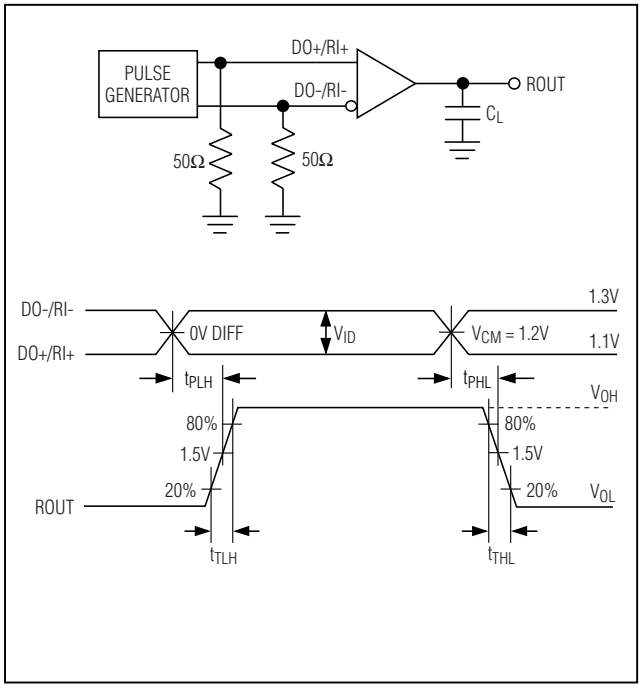


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit and Waveforms

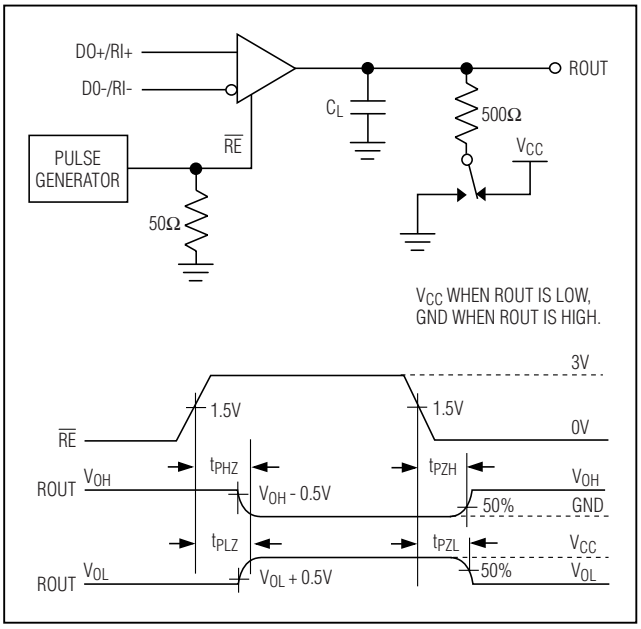
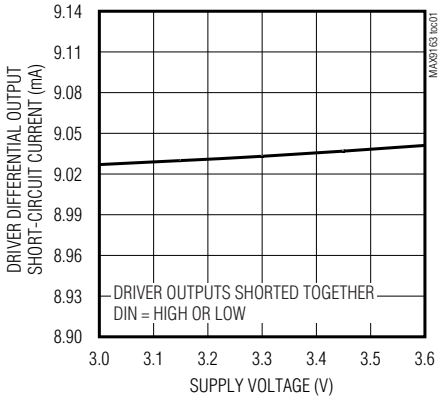


Figure 5. Receiver High-Impedance Delay Test Circuit and Waveforms

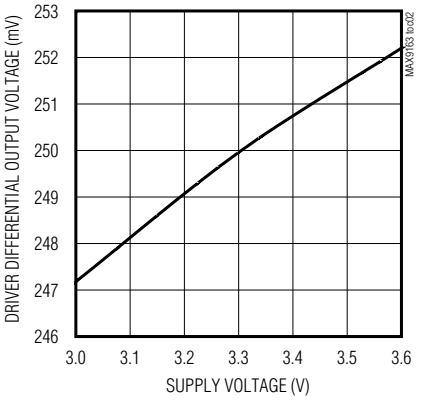
Typical Operating Characteristics

(V_{CC} = 3.3V, FREQ = 100MHz, V_{ID} = 0.2V, V_{CM} = 1.2V, R_L = 27Ω ±1%, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

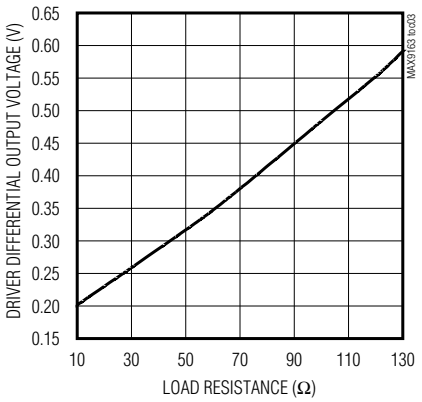
DRIVER DIFFERENTIAL OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE



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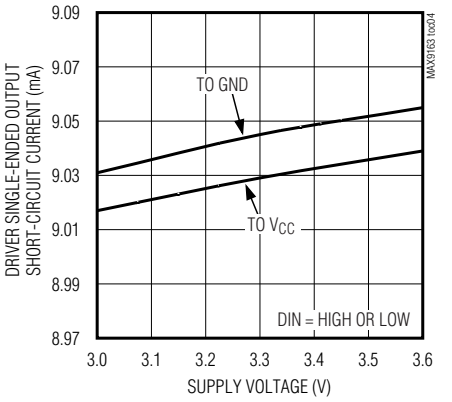
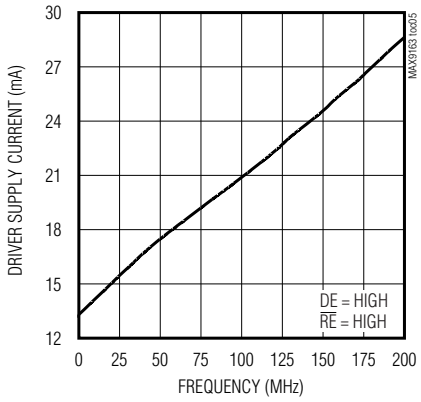
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, FREQ = 100MHz, V_{ID} = 0.2V, V_{CM} = 1.2V, R_L = 27Ω ±1%, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

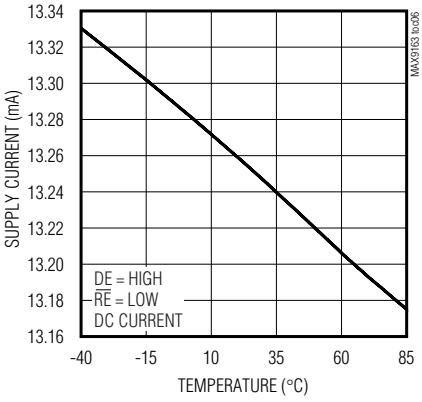
DRIVER SINGLE-ENDED OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAG



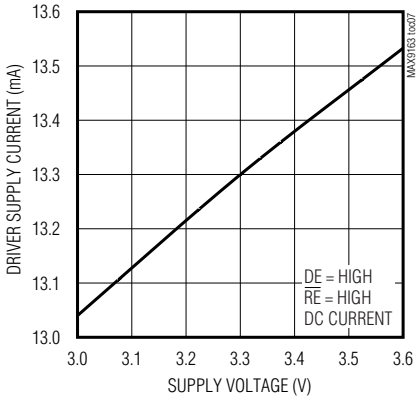
DRIVER SUPPLY CURRENT vs. FREQUENCY



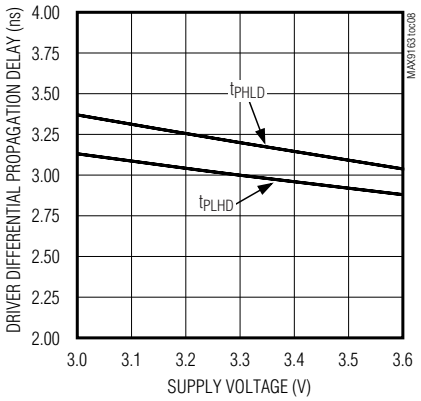
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE



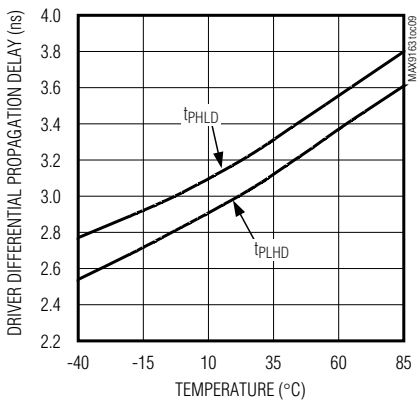
DRIVER SUPPLY CURRENT (I_{CCD}) vs. SUPPLY VOLTAGE



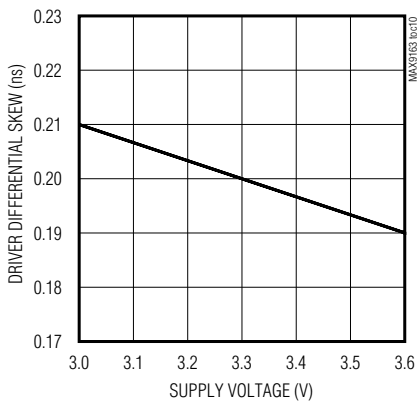
DRIVER DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



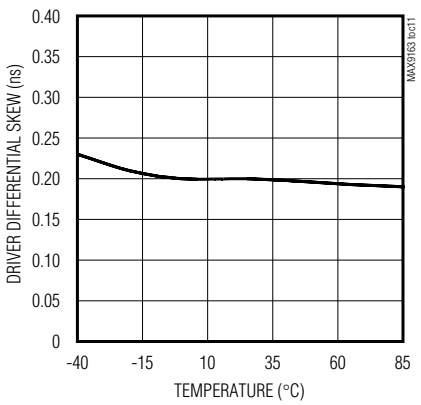
DRIVER DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



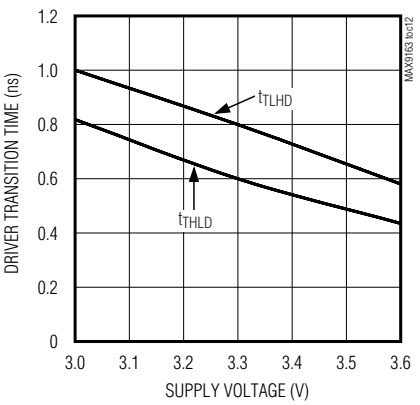
DRIVER DIFFERENTIAL SKEW vs. SUPPLY VOLTAGE



DRIVER DIFFERENTIAL SKEW vs. TEMPERATURE



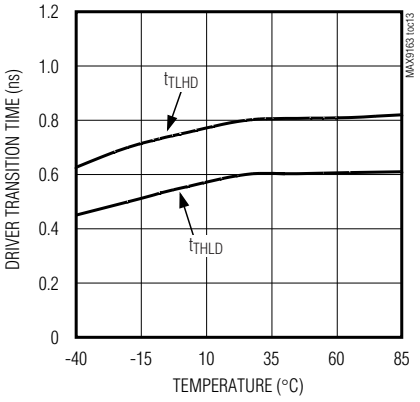
DRIVER TRANSITION TIME vs. SUPPLY VOLTAGE



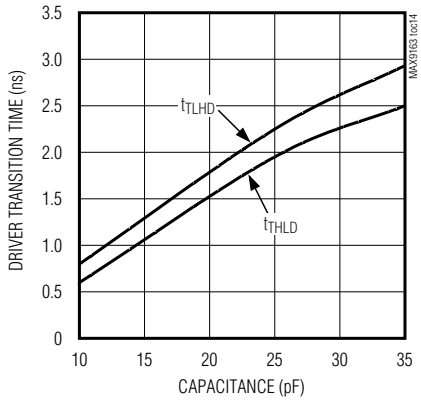
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, FREQ = 100MHz, V_{ID} = 0.2V, V_{CM} = 1.2V, R_L = 27Ω ±1%, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

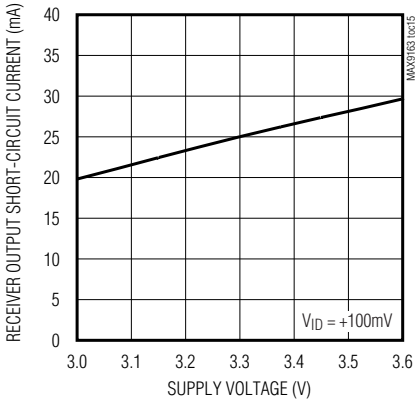
DRIVER TRANSITION TIME vs. TEMPERATURE



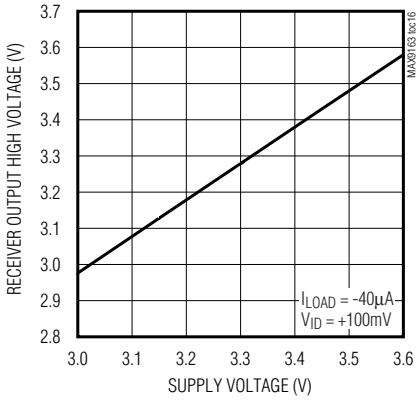
DRIVER TRANSITION TIME vs. TOTAL LOCAL CAPACITANCE



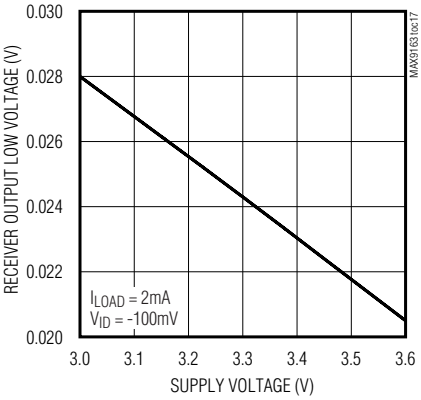
RECEIVER OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



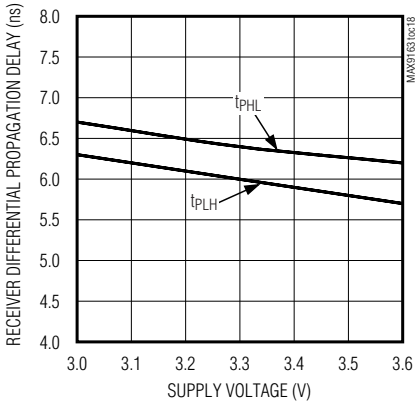
RECEIVER OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



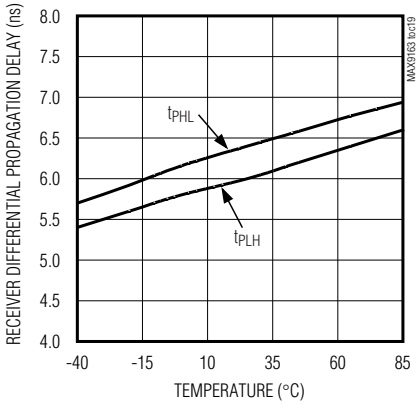
RECEIVER OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



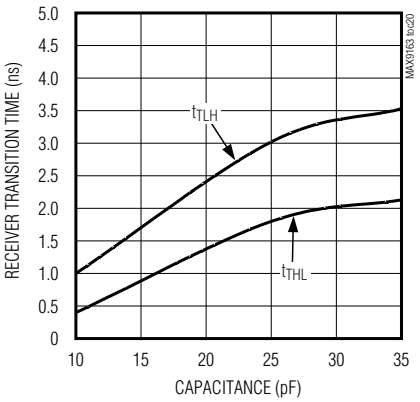
RECEIVER DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



RECEIVER DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



RECEIVER TRANSITION TIME vs. TOTAL LOAD CAPACITANCE



Bus LVDS 3.3V Single Transceiver

Pin Description

PIN	NAME	FUNCTION
1	DE	LVTTL/LVCMOS Driver Enable Input. The driver is enabled when DE is high. When DE is low, the driver output is disabled and is high impedance.
2	DIN	LVTTL/LVCMOS Driver Input
3	ROUT	LVTTL/LVCMOS Receiver Output
4	GND	Ground
5	$\overline{RE}$	LVTTL/LVCMOS Receiver Enable Input. The receiver is enabled when $\overline{RE}$ is low. When $\overline{RE}$ is high, the receiver output is disabled and is high impedance.
6	DO-/RI-	Inverting BLVDS Driver Output/Receiver Input
7	DO+/RI+	Noninverting BLVDS Driver Output/Receiver Input
8	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF ceramic capacitors.

Detailed Description

The MAX9163 high-speed BLVDS transceiver is designed specifically for heavily loaded multipoint bus applications. The MAX9163 operates from a single 3.3V power supply, and is pin compatible with DS92LV010A. The transceiver consists of one differential BLVDS line driver and one LVDS receiver. The driver outputs and receiver inputs are connected internally to minimize bus loading. The driver and receiver can be enabled or disabled individually or simultaneously by the use of enable logic inputs (DE, $\overline{RE}$).

The MAX9163 driver output uses a current-steering configuration to generate a 9mA (typ) output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited. The MAX9163 current-steering output requires a resistive load to terminate the signal and complete the transmission loop. With a typical 9mA output current, the MAX9163 produces a 243mV output voltage when driving a bus terminated with two 54Ω resistors (9mA x 27Ω = 243mV).

The MAX9163 receiver detects a differential input as low as 100mV and translates it to a single-ended output. The device features an in-path fail-safe circuit that sets the receiver output high when the receiver inputs are undriven and open, terminated, or shorted.

Receiver In-Path Fail-Safe

The MAX9163 has in-path fail-safe circuitry, which is designed with a +35mV input offset voltage, a 2.5µA current source between V_{CC} and the noninverting input, and a 5µA current sink between the inverting input and ground (Figure 6). If the differential input is open, the 2.5µA current source pulls the input to about V_{CC} - 0.7V and the 5µA source sink pulls the inverting input to ground, which drives the receiver output high. If the differential input is shorted or terminated with a typical value termination resistor, the +35mV offset drives the receiver output high. If the input is terminated and floating, the receiver output is driven high by the +35mV offset, and the 2:1 current sink to current source ratio (5µA:2.5µA) pulls the inputs to ground. This can be an advantage when switching between drivers on a multipoint bus. The change in common-mode voltage on the MAX9163 is from ground to the typical driver offset voltage of 1.2V. This is less than the change from V_{CC} to 1.2V found on some circuits where the fail-safe circuitry pulls the bus to V_{CC}.

Effects of Capacitive Loading

The characteristic impedance of a differential PC board trace is uniformly reduced when equal capacitive loads are attached at equal intervals (provided that the transition time of the signal being driven on the trace is longer than the delay between loads). This kind of loading is typical of multipoint buses where cards are attached at 1in or 0.8in intervals along the length of a backplane. The reduction in characteristic impedance is approximated by the following formula:

$$Z_{DF\text{-}loaded} = Z_{DF\text{-}unloaded} \times \sqrt{[C_O / (C_O + (N \times C_L / L))]}$$

where:

$Z_{DF\text{-}unloaded}$ = unloaded differential characteristic impedance

C_O = unloaded trace capacitance (pF/unit length)

C_L = value of each capacitive load (pF)

N = number of capacitive loads

L = trace length

For example, if C_O = 2.5pF/in, C_L = 10pF, N = 18, L = 18in, and $Z_{DF\text{-}unloaded}$ = 120Ω, the loaded differential impedance is:

$$Z_{DF\text{-}loaded} = 120\Omega \times \sqrt{[2.5pF / (2.5pF + (18 \times 10pF / 18in))]}$$

where $Z_{DF\text{-}loaded}$ = 54Ω

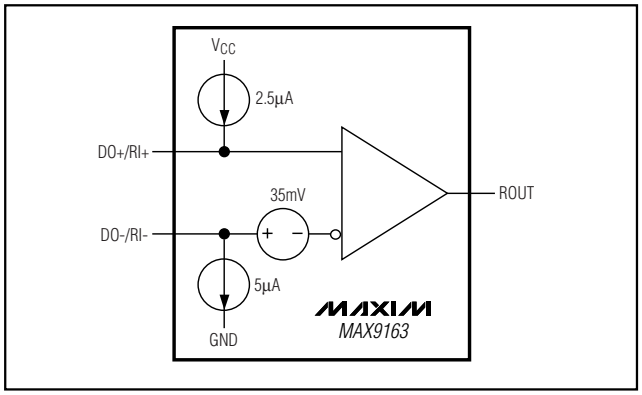


Figure 6. Input Fail-Safe Circuit

In this example, capacitive loading reduces the characteristic impedance from 120Ω to 54Ω. The load seen by a driver located on a card in the middle of the bus is 27Ω because the driver sees two 54Ω terminations in parallel. A typical LVDS driver (rated for a 100Ω load) would not develop a large enough differential signal to be detected reliably by an LVDS receiver.

The MAX9163 BLVDS driver is designed and specified to drive a 27Ω load to differential voltage levels of 180mV to 360mV. A standard LVDS receiver is able to detect this level of differential signal.

Short extensions off the bus, called stubs, contribute to capacitive loading. Keep stubs less than 1in for a good balance between ease of component placement and good signal integrity.

The MAX9163 driver outputs are current-source drivers and drive larger differential signal levels into resistances higher than 27Ω and smaller levels into resistances lower than 27Ω (see the *Typical Operating Characteristics* curves). To keep loading from reducing bus impedance below the rated 27Ω load, PC board traces can be designed for higher unloaded characteristic impedances.

Power-On Reset

The power-on reset voltage of the MAX9163 is typically 2.2V. When the supply falls below this voltage, the device is disabled and the outputs (DO+/RO+, DO-/RO-, and ROUT) are high impedance.

Applications Information

Power-Supply Bypassing

Bypass VCC with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to VCC.

Termination

In the example in the *Effects of Capacitive Loading* section, the loaded differential impedance of the bus is reduced to 54Ω. Because the bus can be driven from any card position, it must be terminated at each end. A parallel termination of 54Ω at each end of the bus placed across the traces provides a proper termination. The total load seen by the driver is 27Ω.

In a multidrop bus where the driver is at one end and receivers are connected at regular intervals along the bus, the bus has lowered impedance due to capacitive loading. Assuming the same impedance as calculated in the multidrop example (54Ω), the multidrop bus can be terminated with a single, parallel-connected 54Ω resistor at the far end of the driver. Only a single resistor is required because the driver sees one 54Ω differential trace. The signal swings are larger with a 54Ω load. In general, parallel terminate each end of the bus with a resistor matching the differential impedance of the bus (taking into account any reduced impedance due to loading).

Traces, Cables, and Connectors

The characteristics of differential input and output connections affect the performance of the device. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the conductors within a differential pair. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between conductors within a differential pair to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Board Layout

For BLVDS applications, a four-layer PC board with separate power, ground, BLVDS, LVDS, and logic signal layers is recommended. Separate the LVTTL/LVCMOS and BLVDS signals to prevent coupling.

Bus LVDS 3.3V Single Transceiver

Typical Application Circuit

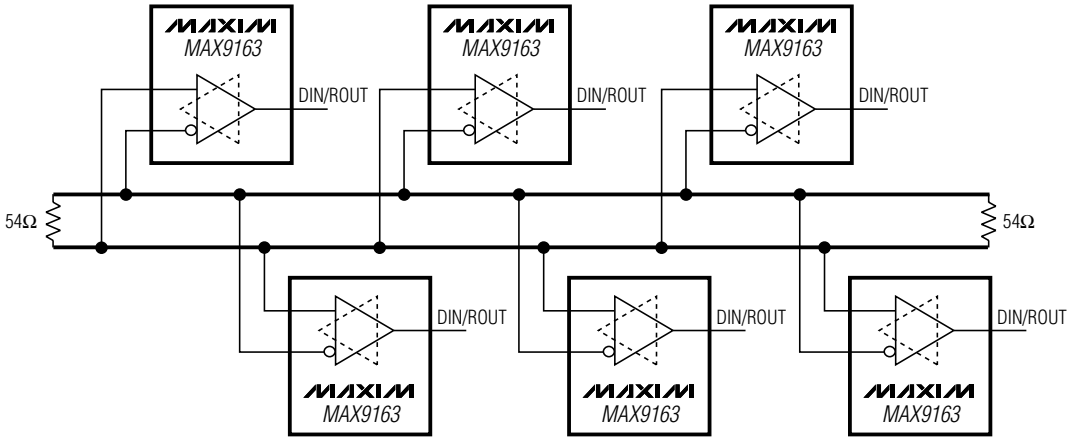


TABLE 1. FUNCTION SELECT

DE	$\overline{RE}$	MODE SELECTED
H	H	Driver
L	L	Receiver
L	H	High impedance
H	L	Loopback

TABLE 2. DRIVER MODE

INPUTS		OUTPUTS	
DE	DIN	DO+/RI+	DO-/RI-
H	L (≤ 0.8V)	L	H
H	H (≥ 2.0V)	H	L
H	(> 0.8mV and < 2.0mV)	Undefined	Undefined
L	X	Z	Z

X: High or low
Z: High impedance

TABLE 3. RECEIVER MODE

INPUTS		OUTPUT
$\overline{RE}$	(DO+/RI+) - (DO-/RI-)	ROUT
L	L (≤ -100mV)	L
L	H (≥ 100mV)	H
L	(> -100mV and < 100mV)	Undefined
L	Undriven and open, shorted, or terminated	H
H	X	Z

DE: Low
X: High or low
Z: High impedance

Chip Information

TRANSISTOR COUNT: 901

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

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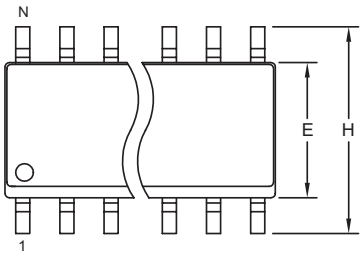
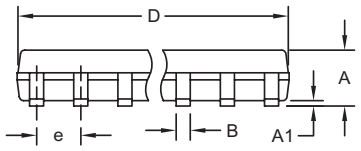


TOP VIEW

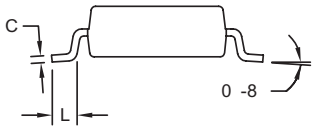
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1